Getting Started With TestSight Tactix
Predictive Fault Spectrum Analysis

Overview

TestSight Tactix provides fast, accurate, comprehensive predictive test coverage analysis of the entire fault spectrum for circuit boards using any combination of ICT, Functional, Boundary Scan, XRay, Optical, and Visual test and inspection methods. The analysis can be completed within minutes of receiving your CAD data, and can be used to determine the effectiveness and completeness of your overall test strategy prior to funding commitments.

Why Predictive Analysis?

Predictive Fault Spectrum Analysis models the effectiveness of a test technology without having to develop the actual test. This dramatically reduces the time and cost of determining whether or not the test technology is cost-effective for a specific circuit board, and whether additional tests should be considered. For predictive analysis purposes, a given test on a tester is rated for effectiveness in detecting one or more of six possible defects for each part, and three possible defects for each pin on a circuit board. The shorthand for this fault spectrum is **PCOA-SOQ-LP**.

The PCOA-SOQ-LP Fault Spectrum

Fault coverage for a circuit board refers to the probability that a tester will detect a fault from the spectrum of all possible faults that can occur. TestSight Tactix uses a PCOA-SOQ-LP circuit board fault spectrum. The model incorporates three fault classes: **1) *part process faults***, **2) *pin process faults***, and **3) *part electrical faults***. The two process classes include faults related to how the circuit board is constructed. The electrical class includes faults related to how the part performs in the circuit.

In the PCOA-SOQ-LP model, P (Present), C (Correct), O (Orientation), and A (Alignment) are *part process faults*. S (Shorts), O (Opens), and Q (Quality) are *pin process faults*. For purposes of the Tactix fault model, pins are defined as any method of part connection to the circuit, including surface mount, thru-hole, press fit, or any other connection method.

The L (Live) and P (Performance) faults are *part electrical faults*. A Live fault occurs when the part is non-operational in the circuit. A Performance fault occurs when the part fails to achieve its designed performance specification. The PCOA-SOQ-LP grouping differentiates process and electrical class faults. This is critical for clearly understanding and applying the model to the wide variety of test technologies being used today.

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The Tactix Test Floor

The Test Floor shows all the testers being used for the entire test process during the production phase being modeled. Multiple test floors can be modeled simultaneously for comparison purposes. The Test Floor grid in the Tactix workspace shows the individual process and electrical class fault coverage percentages for each tester, and the combined percentage for the entire test floor.

Tactix

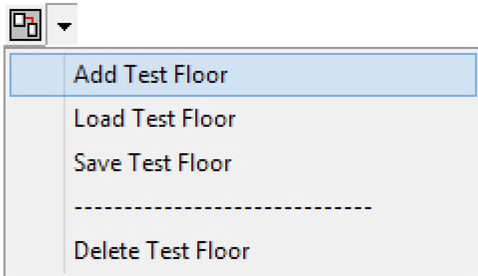
Analysis | DPMO-Sigma | PCOA-SOQ-LP | Both | Test Floor: NPI | List All Testers | No Stress Test

Test Floor | Circuits | Groups | Devices/Packages | Defects | Tests | Current Part | Duplicates

	Testers		Process				Electrical				All		Total				
Test Floor	Tester	Test Plan	P-C-O-A	NT	S-O-Q	NT	Access	Side	L-P	NT	Total	NT	->DPMO	Esc	DPMO->	Sigma	Yield
0	Untested												144757	0	144757	2.6	85.52%
NPI	Agilent AOI	Predictive	74%	0	53%	0	Probes	Any	0%	63	50%	0	144757	489	74360	3	92.56%
	5DX	Predictive	47%	0	100%	0	Probes	Any	0%	63	85%	0	74360	3276	12109	3.8	98.79%
	i3070	Predictive	29%	36	59%	144	Probes	Any	29%	41	53%	36	12109	7	8111	4	99.19%
	Combined		82%	0	100%	0			29%	41	91%	0	144757	328	8111	4	99.19%

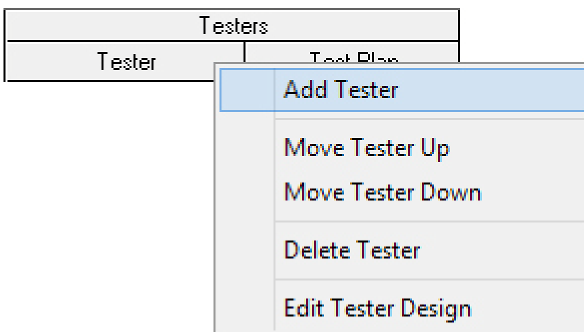
Add a Test Floor

Click on the down arrow of the Test Floor button on the Tactix toolbar and select 'Add Test Floor'.



Add a Tester to the Test Floor

Right-click on the ‘Tester’ column in the ‘Tester’ tab view and select the 'Load Tester' option. This will display all the testers currently in the Tester library.



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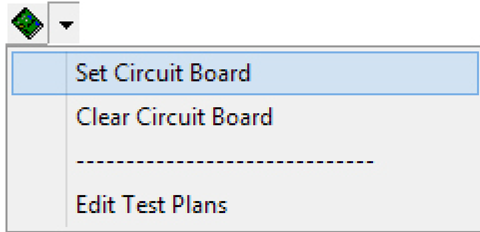
Select a Circuit Board

Select the 'Set Circuit Board' option on the 'Set Analysis Circuit Board' button. Tactix will then run the fault spectrum analysis automatically.



Viewing the Analysis Results

There are various combinations and groupings of parts for easy drill-down to specific areas of interest in the analysis. Parts are grouped by Device (Part Number), Device Type, Package, Package Type, Analog Parts, Non-ByPass Parts, BSCAN Parts, Digital Parts, and ByPass CAPs.

The Tabs in the main Coverage window provide the overview values for each part group. To view the detailed test results for each individual part, select the desired group and defect class by clicking in the P-C-O-A, S-O-Q or L-P field for the group. This will launch the Parts/Pins viewer and automatically list the desired parts.

Test Floor - NPI Part/Pins

Sort Parts Sort Pins List Parts Filter Parts Score Filter Pins Score

List All Testers | List Selected | Agilent AOI - Predictive | List Differences | 5DX - Predictive

Parts | Pins | Summary | Full | Include: ☑ Type ☐ Part Number ☐ Value ☑ PCOA-SOQ-LP ☑ DPMO ☑ Testers ☑ Access ☐ Package ☐ Test Status ☑ Test

All Parts, List All Testers | All Tests | All Test Scores | PCOA 50.2% | LP 9.5% | 63

Sort By Name			Testers			Process								Electrical							DPMO						
Part	Part Type	Pins	Tester	Test Plan	Test	P	C	O	A	Score	S-O-Q	Esc	DPMO->	L	P	Score	Esc	DPMO->	Yield	Total	->DPMO	Esc	DPMO->	Sigma	%DPMO	Access	Comments
C1	CAP	2	Agilent AOI	Predictive	> 0805	F	P	NA	F	0.775	95%	12	182	N	N	0	0	182	99.98%	66.9%	332	12	182	5.1	45.2%		, Value = 0
			5DX	Predictive	> 0805	F	N	NA	F	0.55	100%	2	140	N	N	0	0	140	99.99%	63.8%	182	2	140	5.2	23.1%		, Value = 0
			i3070	Predictive	No Defined Test	N	N	N	N	0	0%	0	140	N	N	0	0	140	99.99%	0%	140	0	140	5.2	0%		No defined test. , Value = 0
					Combined	F	P	NA	F	0.775	100%			N	N	0				69.4%						All	, Value = 0
C2	CAP	2	Agilent AOI	Predictive	> 0805	F	P	NA	F	0.775	95%	12	182	N	N	0	0	182	99.98%	66.9%	332	12	182	5.1	45.2%		, Value = 0
			5DX	Predictive	> 0805	F	N	NA	F	0.55	100%	2	140	N	N	0	0	140	99.99%	63.8%	182	2	140	5.2	23.1%		, Value = 0
			i3070	Predictive	No Defined Test	N	N	N	N	0	0%	0	140	N	N	0	0	140	99.99%	0%	140	0	140	5.2	0%		No defined test. , Value = 0
					Combined	F	P	NA	F	0.775	100%			N	N	0				69.4%						All	, Value = 0
C3	CAP	2	Agilent AOI	Predictive	> 0805	F	P	NA	F	0.775	75%	12	216	N	N	0	0	216	99.98%	56.9%	400	12	216	5.1	46%		, Value = 0
			5DX	Predictive	> 0805	F	N	NA	F	0.55	100%	4	141	N	N	0	0	141	99.99%	63.8%	216	4	141	5.2	34.7%		, Value = 0
			i3070	Predictive	No Defined Test	N	N	N	N	0	0%	0	140	N	N	0	0	140	99.99%	0%	140	0	140	5.2	0%		No defined test. , Value = 0
					Combined	F	P	NA	F	0.775	100%			N	N	0				69.4%						All	, Value = 0
C4	CAP	2	Agilent AOI	Predictive	> 0805	F	P	NA	F	0.775	75%	12	216	N	N	0	0	216	99.98%	56.9%	400	12	216	5.1	46%		, Value = 0

To highlight the score for the parts group in the ViewPort, click directly in the heading for the desired defect class. This will highlight in yellow and display the score in the ViewPort with a color-coded score display.

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The Tester Library

Tactix uses an open rules-based model to determine if a specific test technology can be applied to a defect type on a given part or pin. **See:** Appendix C below for more information on tester modeling.

Tactix includes a library of predefined Tester Models that can be loaded and applied to a circuit board. The models can be easily modified to include or exclude specific test types as needed. For example, if a tester does not have a boundary scan module, you can disable or delete the Scan type tests for the specific tester.

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Appendix A - Definition Of Fault Spectrum Analysis Terms

PCOA-SOQ-LP - The entire defect spectrum for a circuit board

Process Defects - Defects that occur during the construction of the circuit board
Electrical Defects - Defects that occur during power-on operation of the circuit board functions
Defect Class - The groups of part process defects (PCOA), pin process defects (SOQ), part electrical defects (LP)
Weight - The fractional value the defect contributes to the score for a defect class. All weights for the class must sum to 1
Value - The fractional value assigned to a test score
Score - The sum of the test score value times the weight for the defect class

PART PROCESS DEFECTS (PCOA)

PCOA - The percentage score of the process defects for all parts in the group = 100 * SUM(PCOA Scores)/Total Parts

- **Present(P) -** The part is present on the circuit board. Weight = .3
- **Correct(C) -** It is the correct part. Weight = .3
- **Orientation(O) -** The part is placed at the correct angle. Weight =.3
- **Alignment(A) -** The part is properly positioned on the pads. Weight = .1

PIN PROCESS DEFECTS (SOQ)

SOQ - The percentage score of the process defects for all pins in the group = 100 * SUM(SOQ Scores)/Total Pins

- **Shorts(S) -** A pin is shorted to an adjacent pin or pad; weight = .4
- **Open(O) -** A pin is not connected to the circuit board or is internally disconnected; weight = .5
- **Quality(Q) -** Solder joint quality is unreliable; weight = .1

PART ELECTRICAL DEFECTS (LP)

LP - The percentage score of the electrical defects for all parts in the group = 100 * SUM(LP Scores)/Total Parts

- **Live(L) -** The part is electrically alive; weight = .5
- **Performance(P) -** The part meets all design specifications; weight = .5

TOTAL

Total% - The percentage score of all defects for all the parts in the group = 100 * SUM(All Scores) /(2 * Total Parts + Total Pins)

TEST SCORES

Full(F) - The test detects the defect 100% of the time; value = 1
Partial(P) - The test detects the defect 50% of the time; value = .5
None(N) - The test never detects the defect; value = 0
Not Applicable(NA) - The defect does not apply to the part or pin; no value

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Appendix B - Calculating Standard PCOA-SOQ-LP Model Values

For each defect type, a test is rated for effectiveness using three scores: Full, Partial, and None. The corresponding values are 1 for Full, .5 for Partial, and 0 for None. We can interpret these scores as filters that identify all, half, or none of the defects at each test.

Each test applied to a defect class for a part or pin can have a total possible value of 1. Each defect within the class is assigned a weighting factor with all the factors summing to 1. For the **PCOA** class, the weighting factors are P (.3), C (.3), O (.3), and A (.1). For **SOQ**, it is S (.45), O (.45), and Q (.1). For **LP** it is L (.5) and P (.5). The scale can change depending on whether the defect is applicable to a part or pin. Examples of not-applicable (NA) defects include Orientation when applied to a non-polarized part, such as a resistor, and Opens and Quality when applied to a No-Connect pin.

No-Connect Nets

If a pin is a no-connect (NC) pin, then Opens and Quality defects are not applicable since they have no effect on the performance of the part. These defects are scored as not-applicable (NA). The Shorts defect is still considered applicable since it can affect circuit performance.

Appendix C – Predictive Tester Design

The Tester Design for predictive modeling matches a test type to parts that are suitable for the test. There are a wide variety of test types that can be used, but all can be classified as either electrical measurement or observational methods. Observational methods can be XRay or Optical.

Tester Design: i3070

File Library Tester Tests Set Selected Cells Enable Escapes Test Codes

Test Floor | Auditors | Library

Test Floor	Tester Name	Make	Model	Type	Tests	Author	Modified	Description
NPI	Agilent AOI	Agilent	AAOI	Optical	37	DRI	1/20/2014	Scan All Packages
	5DX	Agilent	5DX	XRay	42	DRI	1/20/2014	Scan All Packages
	i3070	Agilent	i3070	ICT	30	DRI	1/16/2014	All 3070 Options, BSDL Loaded

Test Floor: NPI, Tester: i3070

Test Name	Test Type	En	Predictive Qualifier	P	C	O	A	S	O	Q	L	P	Current Part Qualifier
Capacitors	Analog	Yes	Val >= .01nF, Pins <= 3, Any Net Except NC: NA, Access: Electrical All Pins, CAP,	F 1%	P	NA	N	F 1%	F 1%	N	F 1%	P	
Polarized_Cap	Analog	Yes	Val >= .01nF, <= 10uF, Any Net, Access: Electrical All Pins, PCAP	F 1%	P	F 1%	N	F 1%	F 1%	N	F 1%	P	
Resistors	Analog	Yes	Val >= 10 Ohm, Any Net Except NC: NA, Access: Electrical All Pins, RES,	F 1%	P	NA	N	F 1%	F 1%	N	F 1%	P	
Low Value RES	Analog	Yes	Val < 10 Ohm, Any Net, Access: Electrical All Pins, RES, Non-Parallel	F 1%	P	NA	N	F 1%	F 1%	N	F 1%	P	
Parallel Res	Analog	Yes	>= 0.5 of Total Resistance, Any Net, Access: Electrical All Pins, RES, Parallel	F 0%	P	NA	N	F 0%	F 0%	N	F 0%	N	
Parallel Cap	Analog	Yes	>= 0.5 of Total Capacitance, Any Net, Access: Electrical All Pins, CAP, Parallel,	F 0%	P	NA	N	F 0%	F 0%	N	F 0%	N	
ByPass Cap	Analog	Yes	>= 0.5 of Total Capacitance, Any Net, Access: Electrical All Pins, CAP, ByPass,	F 0%	P	F 0%	N	N	N	N	F 0%	N	
Potentiometer	Analog	Yes	Any Net, Access: Electrical All Pins, VRES	F 0%	P	F 0%	N	F 0%	F 0%	N	F 0%	F 0%	
Jumper	Analog	Yes	Pins = 2, Any Net, Access: Electrical All Pins, JUMPER, CONN	F 0%	P	NA	N	F 0%	F 0%	N	F 0%	P	
Diode-LED	Analog	Yes	Any Net Except NC: NA, Access: Electrical All Pins, DIODE, LED	F 1%	P	F 1%	N	F 1%	F 1%	N	F 1%	P	
Zener	Analog	Yes	Any Net, Access: Electrical All Pins, ZENER	F 1%	P	F 1%	N	F 1%	F 1%	N	F 1%	P	

Analog Predictive Test Qualifier: Capacitors

Part Type Match

Type	Name
Part Type	CAP
Part Type	FABCAP
Group	Non-ByPass
Group	Non-Parallel
Part Type	CPCK

Value Match

Type	Units	Match
Value	Farad	>= .01n
Pins	Int	<= 3

Nets Electrical Access Match

Type	Property	Access	Pin Count
Any Net Except NC	NA	Electrical	All Pins

Save Qualifier | Cancel

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Test Qualifier

Tester models contain a series of Tests of specific types depending on the technology being used. Each test has a corresponding Test Qualifier. The Test Qualifier uses three basic match categories to determine if the test should be applied to the part. These are Part Type, Value Match, and Nets Electrical Access Match.

Part Type Match	
Type	Name
Part Type	CAP
Part Type	FABCAP
Group	Non-ByPass
Group	Non-Parallel
Part Type	CPCK

The Part Type Match qualifier can include matches for Part Type, Part Number, Package, Package Type and Group. More than one of any of these match categories can be used for a given test. For the Part Type, Part Number, Package, and Package Type matches, if multiple matches of the same type are include, the match is an OR type, meaning that if any one matches, the part is included. For example, RES and FABRES might be selected for Part Type. If this is the case, it is an OR match, meaning if the part is either a RES or a FABRES it will qualify. If matches of differing types are used, then an AND match is used. For example, if the qualifier includes a Part Type match of RES and a Group match of Parallel, then only parallel resistors will be included in the test.

The Group match list includes Loaded BSDL, BSCAN Tap Port, Non-BSCAN Tap Port, Parallel, Non-Parallel, Bypass, Non-Bypass, Pull Up, and Non-Pull Up. Group matches are AND type. For example, if a Non-Parallel and Non-Pull Up match are included, the part must be both of those to be included in the test.

Value Match

The Value match category provides a mechanism to match specific value properties to a part. The match can be any combination of =, <, or >. The type includes five categories: Value, Pin Count, Pin Pitch, Total Value, and Pins Net Class.

Value Match		
Type	Units	Match
Value	Farad	>= .01n
Pins	Int	<= 3

1. *Value* - used to match part values such as Ohms, Farads, and Henries
2. *Pin Count* - used to match the number of pins on a part
3. *Pin Pitch* - used to match the pitch (separation) between the pins on a part
4. *Total Value* - used in the case of parallel parts; the match value is the percent of the total value represented by an individual part
5. *Pins Net Class* - used to match the percentage of pins on the part that have specific net class selections; three net class types are available: the 'Non Fixed/Gnd/NC' selection means the percentage of pin nets that are not either Fixed, Gnd or NC; the 'Signal Nets' selection means the percentage of pin nets that are Signal class; the 'Critical Nets' selection means the percentage of pin nets that are Critical class

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Nets Electrical Access Match

Nets Electrical Access Match			
Type	Property	Access	Pin Count
Any Net Except NC	NA	Electrical	All Pins

When the tester is an electrical type, it is necessary to determine the access the tester has to a given part for a given test. The Nets Electrical Access Match functionality provides a flexible means to specify minimum access requirements for predictive coverage.

There are six Type selections: *Any Net*, *Net Class*, *BSCAN Pin*, *Enable*, *Any Except Pwr*, *Gnd*, *NC* and *Any Except NC*.

The property setting is not applicable except for Net Class and BSCAN Pin. The Property values for Net Class are: *Signal*, *Clock*, *Fixed*, *Ground*, *NC*, *BSCAN Tap*, *Critical, and True NC*.

The property values for BSCAN Pin are: *Any*, *In*, *Out*, *InOut*, *Buffer*, *TTCK*, *TTMS*, *TTDI*, *TTDO*, *TRST* and *Linkage*.

The Access field determines the type of access the pin must have. The Access values are: *Any*, *Electrical*, *BSCAN Interconnect*, *BSCAN Out*, *BSCAN Interconnect*, *Out*, *Probes/BSCAN Interconnect*, *Probes/BSCAN Interconnect*, *Out*, *TestJet*, *Connects Tap Parts, and Connect To Tap Part*.

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